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Case Docket No. PHD 99,107

THE COMMISSIONER FOR PATENTS, Washington, D.C. 20231

Enclosed for filing is the patent application of Inventor(s):
AXEL HERTWIG; HARALD BAUER; URS FAWER; PAUL LIPPENS

For: MULTIPROCESSOR SYSTEM

ENCLOSED ARE:

[X] Appointment of Associates;
[ ] Information Disclosure Statement, Form PTO-1449 and copies of documents listed therein;
[X] Preliminary Amendment;
[X] Specification (11 Pages of Specification, Claims, & Abstract);
[X] Declaration and Power of Attorney:
(2 Pages of a [ ]fully executed [X]unsigned Declaration);
[X] Drawing (1 sheets of [ ]informal [X]formal sheets);
[X] Certified copy of GERMAN application Serial No.19939763.5;
[X] Authorization Pursuant to 37 CFR §1.136(a)(3)
[ ] Other: ;
[ ] Assignment to .

FEE COMPUTATION

CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE - $690.00
Total Claims	16 - 20 =	0	X $18 =	0.00
Independent Claims	1 - 3 =	0	X $78 =	0.00
Multiple Dependent Claims, if any			$260 =	0.00
TOTAL FILING FEE			=	$690.00

Please charge Deposit Account No. 14-1270 in the amount of the total filing fee indicated above, plus any deficiencies. The Commissioner is also hereby authorized to charge any other fees which may be required, except the issue fee, or credit any overpayment to Account No. 14-1270.

[ ]Amend the specification by inserting before the first line as a centered heading --Cross Reference to Related Applications--; and insert below that as a new paragraph --This is a continuation-in-part of application Serial No. , filed , which is herein incorporated by reference--.

CERTIFICATE OF EXPRESS MAILING

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I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of | Atty. Docket

AXEL HERTWIG ET AL. | PHD 99,107

Serial No. | Group Art Unit

Filed: CONCURRENTLY | Examiner:

Title: MULTIPROCESSOR SYSTEM

Commissioner for Patents
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:

DICRAN HALAJIAN **(Registration No. 39,703)** and

JACK D. SLOBOD **(Registration No. 26,236)**

c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, 580 White Plains Road, Tarrytown, New York 10591, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,

Jack E. Haken, Reg. 26,902
Attorney of Record

Dated at Tarrytown, New York
this 7TH day of August, 2000.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Atty. Docket

AXEL HERTWIG ET AL. PHD 99,107

Serial No.

Filed: CONCURRENTLY

Title: MULTIPROCESSOR SYSTEM

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Claim 3, line 1, delete "or 2".

Claim 4, line 1, change "one of the preceding claims" to --claim 1--.

Claim 5, line 1, change "one of the preceding claims" to --claim 1--.

Claim 6, line 1, change "one of the preceding claims" to --claim 1--.

Claim 8, line 1, change "one of the preceding claims" to --claim 1--.

Claim 9, line 1, change "one of the preceding claims" to --claim 1--.

Claim 11, line 1, change "one of the preceding claims" to --claim 1--.

Claim 13, line 1, change "one of the preceding claims" to --claim 1--.

Claim 14, line 1, change "one of the preceding claims" to --claim 1--.

Claim 15, line 1, change "one of the preceding claims" to --claim 1--.

Claim 16, line 1, change "one of the claims 1 to 15" to --claim 15--.

REMARKS

The claims have been amended to delete multiple dependencies.

The within amendment is limited to the equivalent of cancellation of claims, and pursuant to MPEP §506, should be entered prior to calculation of the fee.

Respectfully submitted,

By _____
Dicran Halajian, Reg. 39.703
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(914) 333-9607
August 5, 2000

Multiprocessor system

The invention relates to a multiprocessor system, more particularly for terminal devices of mobile radiotelephony.

In terminal devices of mobile radiotelephony are used nowadays multiprocessor systems in which two processors are provided on one chip. One processor may be understood to be a system microcontroller which is provided for medium-power protocol and control tasks, whereas the other processor may be a powerful digital signal processor. For each processor there is at least one memory external to the chip, thus for example an external FLASH program memory, or a respective external data memory. In this system a certain memory is assigned to only one processor, that is to say, only this processor can access the defined memory. Such a system configuration, however, is disadvantageous in various respects. The respective chip is to be provided with a plurality of pins for the communication of the various chips included in the processors, on the one hand, and the separate memories, on the other. Furthermore, the power consumption for the program and data communication is considerably large. The described configuration also requires considerably much space, which is a disadvantage especially in the terminal devices which become ever smaller.

For this purpose, the invention has for its object to provide a multiprocessor system which in the area of telecommunications technique and, more particularly, in terminal devices of mobile radiotelephony, is improved in comparison with the state of the art.

For solving this problem in a multiprocessor system, more particularly for terminal devices of mobile radiotelephony, the following is arranged on a common chip:

- at least two processors,
- at least one rewritable memory to which the two processors can have access,
- at least one cache memory via which the first processor has access to the memory, and
- at least one bridge via which the second processor has access to the memory.

In the processor system according to the invention, the processors and also at least one rewritable memory to which the two processors can have access and can extract or write respective information, are advantageously integrated on a common chip. The first processor, which may be, for example, a digital signal processor, is connected to the

rewritable memory via at least one cache memory. The access of the second processor, which may be a system microcontroller, is realized via at least one bridge. According to the invention the integration of said elements on a common chip enables a communication between the processors and the memory on the chip and, since the memory is not an external memory, no pins can be provided at all. The integration rate of the chip is increased considerably. The current necessary for the communication between the processors and the memory is considerably less too, because a chip-integrated memory generally optimizes the power consumption of a system. The system architecture described may be used, more particularly, in terminal devices of mobile radiotelephony in the GSM standards DCS1800, PCS1900, IS95 and IS136.

The two processors can work with mutually different operating rates. Furthermore, there may be provided that the memory is connected to the first processor via two cache memories, one of which is used for access to the memory for reading or writing a program and the other of which is used for access to the memory for reading out data. The non-volatile rewritable memory thus has various memory areas in which different information can be stored. Program and data for each of the connected processors may be stored freely in the non-volatile rewritable memory. Via the two cache memories, which are high-speed buffers, there is ensured that the data or information to be retrieved from the relatively slowly operating memory are available to the high-speed first processor or the digital signal processor respectively. The two cache memories further enable a simple access of the second processor (for example, microcontroller) to the memory, because it is ensured via the cache memory that the first processor (for example, digital signal processor) does not continuously retrieve data from the memory and occupies this memory because the essential data needed by the first processor or the digital signal processor respectively, usually have already been stored in the two cache memories and are retrieved from there, so that the memory is not continuously occupied by the first processor and also the second processor can access the memory via the bridge.

As has been described, the memory is advantageously subdivided into separate memory areas for a program and for data. The respective processors may then be assigned separate memory areas for programs and for data, that is to say, for example two program areas are available of which one area is assigned to the first processor or digital signal processor respectively, and the other area is assigned to the second processor or system microcontroller respectively, as also respective data memory areas are provided. All in all, this provides the possibility of partitioning the memory areas as desired. However, it is

necessary to determine the total required memory space before a first implementation; the partitioning may then be set at will. Obviously, it is also possible to provide a further memory area for data which can be accessed by the two.

In a further embodiment of the invention the bridge may be arranged for the synchronization between a first data bus by which the memory communicates, and a second data bus by which the second processor communicates, and which is narrower as regards the transmission width. The complete integration of the said system components on a chip enables the formation of data buses in a simple manner. Since the integrated memory is to effect high transmission rates especially in the scope of the communication with the first processor or the digital signal processor respectively, it is efficient to assign to this integrated memory a data bus having a large transmission width via which the data can be delivered to the first processor that works with a high clock frequency. Since the second processor works with a lower clock and, therefore, more slowly, it is sufficient to assign a data bus having a lower transmission rate to this second processor. However, since the second processor can now also access the rewritable memory, it is necessary to accordingly synchronize the information to the second data bus via the first data bus, which is done in a simple manner by means of the bridge. It has proved to be efficient for the data bus assigned to the memory to have a transmission width of 128 bits and for the data bus assigned to the second processor to have a transmission width of 32 bits.

As described, the use of the cache memory (memories) achieves that the first processor or the digital signal processor respectively, does not continuously occupy the rewritable memory or the data bus assigned thereto, it is rather a discontinuous access to the memory, only when new information is to be loaded into the cache memory (memories). If, nevertheless, there were an access conflict when at the same time also the first processor would like to access the memory, this conflict would be solved according to the invention by means of the bridge which is arranged for managing the access to the memory, so that in the case of a conflict of access preferably the first processor is served, because this processor generates the larger load and is to satisfy the stricter real-time requirements. The bridge is thus arranged both for synchronization and for arbitration.

For storing mainly volatile variable data, it has proved to be efficient when a further chip-integrated data memory is connected to the second processor via a data bus. In this data memory are stored short-term data, for example, computed data which will soon be overwritten again. For enabling also the first processor or the digital signal processor respectively to access the further data memory, according to the invention a DMA controller

and also a second bridge can be integrated on a chip. The combination of the DMA controller and the second bridge enables in a simple manner the access to the relatively slowly operating further data memory. All in all, this embodiment now provides a system with various processors and various memories integrated on a common chip, each processor being capable of accessing each memory, so that an extremely functional information transfer and operation is made possible.

Furthermore, it has proved to be advantageous when at least an internal high-speed data memory and/or at least an internal high-speed program memory is assigned to the first processor. In these high-speed memories are preferably stored time-critical program portions, which are immediately to be available to the first processor or the digital signal processor respectively, or modifiable variable data which are also to be available immediately. The first processor can in this context have a double Harvard architecture in which each provided data or program memory is assigned its own bus for data words or program words.

The rewritable memory can, according to the invention, be an MTP memory (Multiple Programmable Memory) or a FLASH memory. The further data memory in the second processor may be a DRAM (Direct Random Access Memory) or a SRAM (Static Random Access Memory). The internal high-speed data memory and/or the internal high-speed program memory may be a RAM. Furthermore, there may also be provided a direct communication link between the two processors.

As a result of the multiprocessor system according to the invention there are many advantages over the state of the art. On the one hand, the partitioning between the processors and between program area and data area inside the integrated rewritable memory can be changed at will, as described, only the total memory capacity of the system is to be definite when the chip is manufactured. Due to the possibility of rewriting the memory in which the program for operating the respective device is stored, new software versions both for the system controller and for the signal processor can be loaded in a simple and high-speed manner. The integration of the memory (various memories) on the chip optimizes the power consumption of the system and reduces the number of pins on the housing of the chip or allows the available pins to be occupied differently. This leads to a saving of cost and space. As a result of the mechanisms to access the memories, the dimensioning of the cache memories and of the local memories, the slightly longer time of access to the rewritable memory is compensated in a simple manner at the least cost. Finally, the combination of a plurality of memories or the individual partitioning and distribution of the memory areas in

the rewritable memory integrated on a chip reduces the implementation overhead and the necessary chip surface.

Besides the multiprocessor system itself, the invention further relates to a utilization of the multiprocessor system of the type described above for operating a telecommunication terminal of mobile radiotelephony.

Further advantages, features and details of the invention will be apparent from the example of embodiment described hereinafter and from the drawing.

The Figure shows in the form of a basic circuit diagram the elements configured or integrated respectively on a chip, which is not further shown. A first processor 1 is shown in the form of a digital signal processor 2 (DSP). The digital signal processor 2 is a powerful processor having an output of 25-100 MIPS (Millions of Instructions Per Second). In the processor sub-system 3, represented by the box shown in the Figure, is further provided an internal high-speed program memory 4 in the form of an integrated RAM in which time-critical program portions are stored which are briefly necessary for the signal processor. Furthermore, two integrated high-speed data memories 5 are provided for storing volatile short-term data. Separate buses 6a, 6b, 6c having a transmission rate of 16 bits each are assigned to the memories 4, 5. Via these buses the signal processor 2 communicates with the respective memories. The program memory 4 may have a storage capacity of, for example, 2×16 k with a transmission width of 16 bits, the data memory 5 may be designed to have a storage capacity of 8×16 k and a transmission width of 16 bits. Furthermore, the processor sub-system 3 includes a plurality of input and output units 7 via which, on the one hand, data can be output from the data memories 5 and can be input to them respectively, and also data from a further data memory which will be described hereinafter.

To the digital signal processor 2 or the processor sub-system 3 respectively are assigned two cache memories 8, 9 via which the digital signal processor 2 can access a rewritable memory 10 also integrated on the chip, which memory 10 is arranged as an MTP memory in the example shown. The communication between the cache memories 8, 9 and the rewritable memory 10 is effected via a data bus 11 which has a preferred transmission width of 128 bits. The memory 10 is subdivided into different memory areas while there is a possibility of writing or reading out, on the one hand, a program and, on the other hand, the constant data. Each area is in its turn subdivided and assigned either to the digital signal processor 2 or to a second processor 12 in the form of a system microcontroller 13 (μC) which, as will be further described hereinafter, also has access to the memory 10. The access to the program values takes place via the cache memory 8, the access to the data words via

the cache memory 9. By means of the cache memories, which work as high-speed buffer memories, there is ensured that the digital signal processor 2 does not continuously occupy the data bus 11, the necessary data are rather read from the cache memories 8, 9 in which the necessary information is buffered. The cache memories 8, 9 communicate with the digital signal processor via the respective buses 6a, 6b and 6c. Conditional to this communication link it is also possible to output words from the memory 10 or the cache memories 8, 9 respectively via the output units 7. The memory 10 is to have a storage capacity of at least 0.5-2 megabytes with a transmission width of 128 bits. Obviously it is alternatively possible to dimension them larger. The cache memories, in the case of the cache memory 8, may have a capacity of 512 bytes, the capacity of the cache memory 9 may be 64 bytes.

As already described, the chip further accommodates a second processor in the form of a system microcontroller 13. Assigned to this microcontroller is a second data bus 14 which has a transmission width of 32 bits. To enable the system microcontroller 13 to access the relevant program and data portions relevant to it in the memory 10, a bridge 15 is provided via which the system microcontroller 13 can have access via the data bus 14. The bridge is used, on the one hand, for the synchronization between the two data buses 11, 14 because the two work with different clocks – as do the digital signal processor 2 and the system microcontroller 13 – which is denoted by the dashed line "clock separation". The digital signal processor and all the components assigned thereto work with a working clock pulse of, for example, 26-104 MHz, whereas the system microcontroller and the respective elements assigned thereto work with a working clock pulse of, for example, 26 MHz. In addition, the bridge 15 also takes over arbitration tasks, so that it always permits the digital signal processor 2 or cache memory 8, 9 to have preferred access to the memory 10. Furthermore, there is a possibility of using the bridge 15 as a small cache memory, so that fewer memory accesses from the side of the system microcontroller to the memory 10 are necessary. In this manner, also any possible waiting cycles with respect to the system microcontroller accessing the memory are shortened.

To the system microcontroller 13 is further assigned a further data memory 16 in the form of a DRAM or SRAM integrated on the chip. This data memory may have a capacity of 32 k with a transmission width of 32 bits on the data bus 14. The system microcontroller 13 has immediate access to the further data memory 16. In order to also enable the digital signal processor 2 to have access to the further data memory in which volatile short-term data are stored, a DMA controller 17 is provided which is also connected to the data bus 14, and a further bridge 18 which is connected to the sub-system internal bus

6c. It is true, the further data memory 16 works very slowly compared to the high clock frequency of the digital signal processor 2, as a result of which it will rarely be accessed. This access, however, is possible by means of the DMA controller 17 and the bridge 18, which bridge is again arranged for the synchronization between the different data buses and the clock frequencies.

To the data bus 14 is further connected a boot ROM 19 via which the original configuration of the memory 10 and the original inputting of the program and possible data is effected.

Furthermore, various peripheral elements 21 integrated on a chip, such as interfaces to external components or the like, are connected via a third bridge 20. Besides, via a respective terminal device 22, a chip-external further memory, for example a FLASH memory can be connected. This FLASH memory is used for extending the memory 10 integrated on the chip when its memory capacity is no longer sufficient. The external memory is connected as an input/output unit of the system microcontroller 13. The digital signal processor 2 can access this external memory via the DMA controller 17 and the bridge 18.

It is obvious that the said memory dimensioning and the design of the transmission rates and the transmission widths of the data buses used may be changed in dependence on the respective application.

CLAIMS:

1. A multiprocessor system more particularly for terminal devices of mobile radiotelephony in which are arranged on a common chip:

- at least two processors (1, 12),
- at least one rewritable memory (10) to which the two processors (1, 12) can have access,
- at least one cache memory (8, 9) via which the first processor (1) has access to the memory (10), and
- at least one bridge (15) via which the second processors (12) has access to the memory (10).

2. A multiprocessor system as claimed in claim 1, characterized in that the two processors (1, 12) work with mutually different working clocks.

3. A multiprocessor system as claimed in claim 1 or 2, characterized in that the first processor (1) is a digital signal processor (2) and the second processor (12) is a system microcontroller (13).

4. A multiprocessor system as claimed in one of the preceding claims, characterized in that the memory (10) is connected to the first processor (1) via two cache memories (8, 9), one of which is used for access to the memory (10) for reading a program and the other of which is used for access to the memory (10) for reading out data.

5. A multiprocessor system as claimed in one of the preceding claims, characterized in that in the memory (10) each processor (1, 12) is assigned a separate memory area for a program and for data.

6. A multiprocessor system as claimed in one of the preceding claims,

characterized in that the bridge (15) is provided for synchronization between a first data bus (11) via which the memory (10) communicates, and a second data bus (14) via which the second processor (12) communicates and which has a narrower transmission width.

7. A multiprocessor system as claimed in claim 6, characterized in that the data bus (11) assigned to the memory (10) has a transmission width of at least 128 bits and the data bus (14) assigned to the second processor (12) has a transmission width of at least 32 bits.

8. A multiprocessor system as claimed in one of the preceding claims, characterized in that the bridge (15) is provided for managing the access to the memory (10) so that in the case of a conflict of access, preferably the first processor (1) is served.

9. A multiprocessor system as claimed in one of the preceding claims, characterized in that a further data memory (16) integrated on a chip is connected to the second processor (12) via a data bus.

10. A multiprocessor system as claimed in claim 9, characterized in that for enabling an access of the first processor (1) to the further data memory (16) on the chip a DMA controller (17) and a second bridge (18) are provided.

11. A multiprocessor system as claimed in one of the preceding claims, characterized in that the first processor (1) is assigned at least an internal high-speed data memory (5a, 5b) and/or at least an internal high-speed program memory (4).

12. A multiprocessor system as claimed in claim 11, characterized in that the processor sub-system (3) formed by the first processor (1) and the internal memory (memories) has a double Harvard architecture.

13. A multiprocessor system as claimed in one of the preceding claims, characterized in that the memory (10) is an MTP memory or a FLASH memory.

14. A multiprocessor system as claimed in one of the preceding claims,

characterized in that the further data memory (16) of the second processor (12) is a DRAM or SRAM.

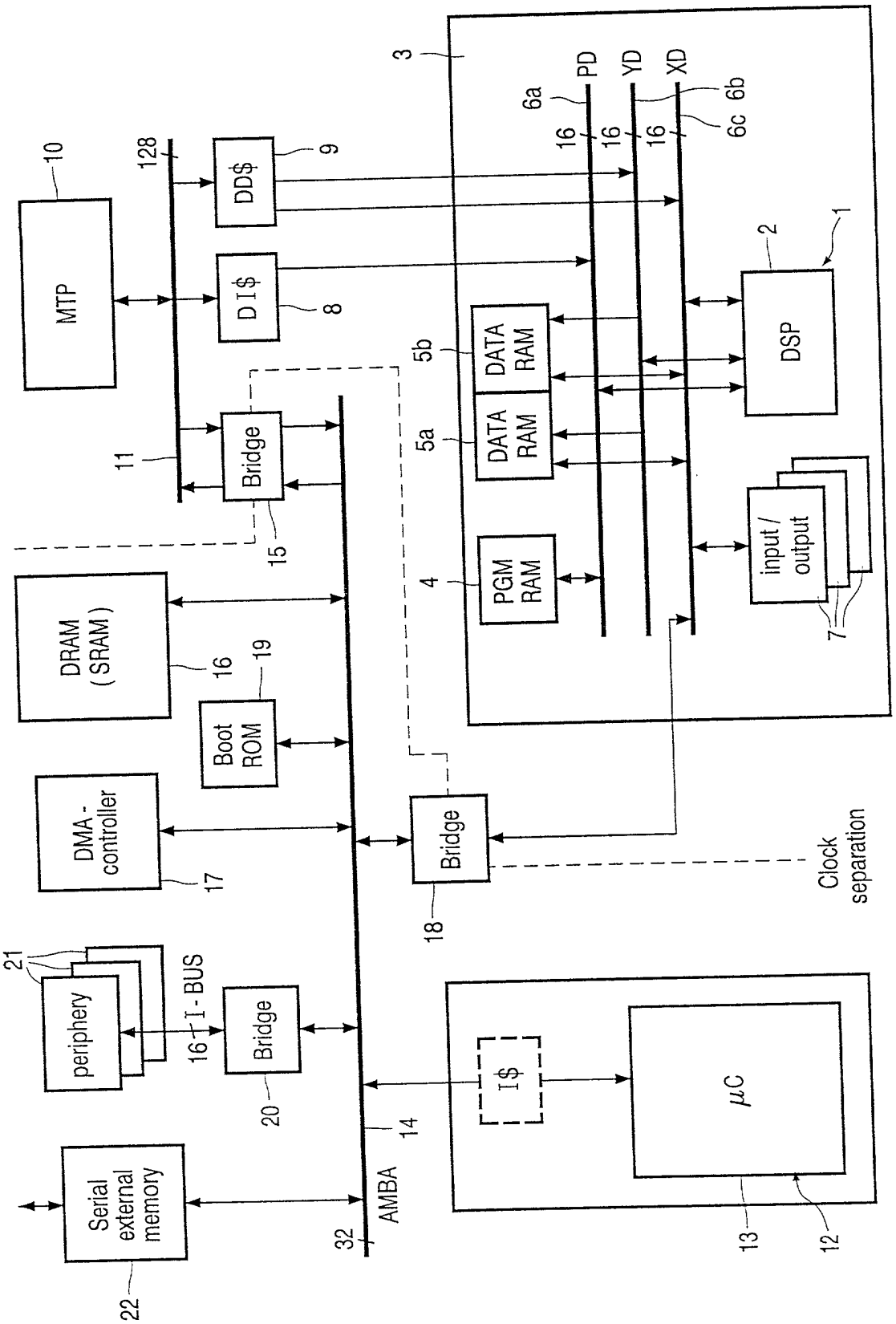
15. A multiprocessor system as claimed in one of the preceding claims, characterized in that the internal high-speed data memory (5a, 5b) and/or the program memory (4) is a RAM.

16. A use of a multiprocessor system as claimed in one of the claims 1 to 15 for the operation of a telecommunication terminal device of mobile radiotelephony.

ABSTRACT:

A multiprocessor system, more particularly for terminal devices of mobile radiotelephony, in which system are arranged on a common chip:

- at least two processors,
- at least one rewritable memory which can be accessed by the two processors,
- at least one cache memory via which the first processor has access to the memory,
- at least one bridge via which the second processor has access to the memory.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Clock separation
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DECLARATION and POWER OF ATTORNEY

ATTORNEY'S DOCKET NO.:
PHD 99.107 US

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **"Multiprocessor system"**

the specification of which (check one)

☐ is attached hereto.

☐ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by the amendment(s) referred to above.

I acknowledge the duty to disclose information which is material to patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

COUNTRY	APP. NUMBER	DATE OF FILING (DATE, MONTH, YEAR)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Germany	**19939763.5**	**21 August 1999**	**YES**

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1,56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PRIOR UNITED STATES APPLICATION(S)

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Algy Tamoshunas, Reg. No. 27,677
Jack E. Haken, Reg. No. 26,902

SEND CORRESPONDENCE TO: Corporate Patent Counsel;	DIRECT TELEPHONE CALLS TO:
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Dated:		Inventor's Signature:		
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Residence & Citizenship	City	State of Foreign Country	Country of Citizenship	
Post Office Address	Street	City	State of Country	Zip Code
Dated:		Inventor's Signature:		
Full Name of in Inventor	Last Name	First Name	Middle Name	
Residence & Citizenship	City	State of Foreign Country	Country of Citizenship	
Post Office Address	Street	City	State of Country	Zip Code
Dated:		Inventor's Signature:		
Full Name of in Inventor	Last Name	First Name	Middle Name	
Residence & Citizenship	City	State of Foreign Country	Country of Citizenship	
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